**MNP V3 ACM SPECIFIC STM32MP1 GPI0s (Rev E)**

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| # | Ball | GPIO PORT | SIGNAL NAME | DIR | DESCRIPTION |
| 1 | AA8 | PB5 | RS485\_1\_RX | I | Reader Port 1 OSDP RS485 Receive (UART5) |
| 2 | W13 | PB6 | RS485\_1\_TX | O | Reader Port 1 OSDP RS485 Transmit (UART5) |
| 3 | E14 | PC8 | RS485\_1\_DE | O | Reader Port 1 OSDP RS485 Data Enable (UART5)  High – RS485 Port 1 Transmitter Enabled.  Low --. Disabled |
| 4 | AA7 | PB12 | RS485\_1\_TE | O | Reader Port 1 OSDP RS485 Terminator Enable  High --- RS485 Terminator Enabled; Port 1 in OSDP Mode  Low ---- Terminator Disabled; Port 1.in Wiegand Mode |
| 5 | AB11 | PF9 | WGD1\_D0\_3V3 | I | Reader Port 1 Wiegand Data 0 |
| 6 | B6 | PK3 | WGD1\_D1\_3V3 | I | Reader Port 1 Wiegand Data 1 |
| 7 | B3 | PH11 | WGD1\_BPR | O | Reader Port 1 Beeper. High True |
| 8 | Y1 | PC2 | WGD2\_D0\_3V3 | I | Reader Port 2 Wiegand Data 0 |
| 9 | C7 | PJ15 | WGD2\_D1\_3V3 | I | Reader Port 2 Wiegand Data 1 |
|  | B8 | PJ12 | WGD2\_BPR | O | Reader Port 2 Beeper. High true |
| 10 | C5 | PE0 | RS485\_2\_RX | I | Reader Port 2 OSDP RS485 Receive. (UART8) |
| 11 | D7 | PE1 | RS485\_2\_TX | O | Reader Port 2 OSDP RS485 Transmit (UART8) |
| 12 | B4 | PE14 | RS485\_2\_DE | O | Reader Port 2 OSDP RS485 Data Enable (UART8)  High – RS485 Port 2 Transmitter Enabled.  Low --. Disabled |
| 13 | E4 | PE12 | RS485\_2\_TE | O | Reader Port 2 OSDP RS485 Terminator Enable  High --- RS485 Terminator Enabled; Port 2 in OSDP Mode  Low ---- Terminator Disabled; Port 2 in Wiegand Mode |
| 14 | V12 | PF10 | LADR0 | O | RLY Enable/WGD LED Latch Address 0 |
| 15 | Y11 | PG7 | LADR1 | O | RLY Enable/WGD LED Latch Address 1 |
| 16 | C6 | PK5 | LADR2 | O | RLY Enable/WGD LED Latch Address 2 |
| 17 | B7 | PJ14 | LDAT | O | RLY Enable/WGD LED Latch Data  High --- Addressed Latch ON  Low ---- Addressed Latch OFF |
| 18 | AA9 | PG10 | LEN\_L | O | RLY Enable/WGD LED Latch Enable  Low True. Data latched on rising edge |
| 19 | AB8 | PB8 | STRIKE1\_KICKER\_EN | O | Output Relay 3 Enable 28V Supply, Kick voltage for WET Mode  28V pulse for 24V strikes only. High True |
| 20 | AB10 | PF8 | SPARE\_GPIO\_1 | I/O | SPARE . GPIO routed to (R578) |
| 21 | W6 | PF15 | STRIKE2\_KICKER\_EN | O | Output Relay 4 Enable 28V Supply, Kick voltage for WET Mode  28V pulse for 24V strikes only. High True |
| 22 | Y6 | PH3 | SPARE\_GPIO\_2 | I/O | SPARE. GPIO routed to (R582) |
| 23 | R4 | ANA0 | IN1\_ADC | I | Input 1: Analog input voltage **Note: ALL ADC Inputs are to be**  **connected to the same STM32MP1 ADC ( 1or 2)** |
| 24 | T5 | ANA1 | IN2\_ADC | I | Input 2: Analog input voltage |
| 25 | W8 | PF11 | IN3\_ADC | I | Input 3: Analog input voltage |
| 26 | V8 | PF12 | IN4\_ADC | I | Input 4: Analog input voltage |
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| # | **Ball** | **GPIO PORT** | **SIGNAL NAME** | **DIR** | **DESCRIPTION** |
| 27 | A9 | PD5 | nPoEP\_PSE | I | POE Plus signature detected from PSE. Low True |
| 28 | D8 | PK0 | nPoE\_PSE | I | POE signature detected from PSE. Low True |
| 29 | E13 | PC6 | LED\_POE | O | Status LED: Node Powered by POE. High True |
| 30 | C9 | PD4 | LED\_POEP | O | Status LED: Node Powered by POE Plus. High True |
| 31 | AA11 | PF6 | M4\_RUN\_L | O | Status LED for Co-Processor (M4) Running. Low True |
| 32 | F14 | PC10 | FRAM\_POP\_L | I | FRAM Populated vs Batt Backup SRAM; Low True. |
| 33 | AA10 | PF7 | INSTALLED\_RSVD | I | Reserved HW Configuration bit |
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|  |  |  | **REASSIGNED GPIO** |  |  |
| 1 | K5 | PZ2 | CPU\_SPI1\_D1 | I/O | (SRAM\_SPI\_MOSI) Reassigned to resolve GPIO conflict with. Was at U501-AA8 |
|  |  |  | **GPIO Direction Change** |  |  |
|  | V4 | PA1 | CPU\_REFCLK | I | GPIO changed to Input. External 50Mhz clock. New RMII clock configuration |
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